Notice of Allowability	Application No.	Applicant(s)	
	10/643,188	HAZAMA, KATSUKI	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/19/03*.

2. ☒ The allowed claim(s) is/are *37-42 (now renumbered 1-6)*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *08/931519* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 8/19/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *6/19/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Noel Kiviln on 6/19/06.

The application has been amended as follows:

Claim 37 line 3 as presented:

"so as to correspond to a physical addresses converted from"

Claim 37 line 3 as amended:

"so as to correspond to a physical addresses converted from"

Claim 40 line 3 as presented:

"so as to correspond to a physical addresses converted from"

Claim 40 line 3 as amended:

"so as to correspond to a physical addresses converted from"

Please amend the title as follows:

~~Multilevel Semiconductor Memory, Write/Read Method Thereto/Therefrom And Storage Medium Storing Write/Read Program~~ System and Method For Reading Data Stored In A Semiconductor Device Having Multilevel Memory Cells

Please amend the Abstract as follows.

A semiconductor device has multilevel memory cells, each cell storing at least three levels of data each. ~~At least a first data composed of first data bits and a second data composed of second data bits are arranged in order that at least a bit of an N-order of the first bits and a bit of the N-order of the second bits are stored in one of the cells, the N being an integral number. A voltage corresponding to the N-order bits is generated and applied to the one of the cells in response to an address information corresponding thereto. Another semiconductor device has~~ The multilevel memory cells are arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by n ($n \geq 2$) number of bits (X1, X2, . . . , Xn). A logical address is converted into a physical address of the physical address space. ~~Judging~~ A judgement is made as to whether a logical address space including the logical address matches the physical address space. When matched, the most significant bit X1 is specified ~~once using~~ by performing a single comparison operation using a reference value. The specified bit is output from one of the cells corresponding to the physical address. If not matched, the bits (X2, . . . , Xn) are specified by ~~n-time specifying operation maximum using maximum n number of~~ performing multiple comparison operations using different reference values~~. The data writing/reading operations to/from the semiconductor devices can be stored in a computer readable medium as program codes for causing a computer to execute these operations~~.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

The present invention pertains to a multilevel memory device having a method of testing the device and computer readable medium storing program code to implement the method.

The claimed invention (claim 39 as representative being the broader of the independent claims) recites features such as: "...preparing a judging value for specifying at least one of the data components; and applying a voltage corresponding to the judging value to the control gate to determine whether a current flows between the source and the drain when the logical address is included in an address space A1 that corresponds to an address space including the physical address."

The prior arts of record (Barth, U.S. Patent No. 5,943,693 as an example of such prior arts) teach a memory addressing circuitry for accessing an n-dimensional memory system which includes address translation circuitry for translating logical addresses into physical address corresponding to storage locations which are separated by a constant number of rows and/or columns. The column, row, and level spacing factors are chosen such that the columns are physically distinct, the rows are physically distinct, and the storage locations do not share a same memory cell. The prior arts however do not teach the claimed method of "...preparing a judging value for specifying at least one of the

data components; and applying a voltage corresponding to the judging value to the control gate to determine whether a current flows between the source and the drain when the logical address is included in an address space A1 that corresponds to an address space including the physical address."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138